Tropical Assemblies Suggested Design for Manufacturability Overview:

The guidelines below can help you standardize the fabrication and assembly of your product, while lowering its cost. These guidelines do not represent TAI's full capabilities (such as smallest hole size, tightest spacing, and so forth). Rather, they indicate the tightest tolerance for which optimum pricing can be provided. The layout guidelines, when followed, will reduce or eliminate the need for non-standard processes and their associated costs.

Surface Mount Technology

I. Component-side (Top) vs. Wave-side (Bottom) Placement

A. It is preferable to place all complex surface mount technology (SMT) components on the component-side of the board.
   1. Examples of complex SMT components are QFPs, BGAs and TSOPs.

B. If necessary, discrete components can be placed on the wave-side (bottom) of the board.
   1. Examples of discrete components are chip resistors, chip capacitors and small outline diodes (SOD).
   2. Components should be oriented in the same direction (perpendicular to the length of the assembly) for optimal wave soldering.

C. The following SMT components are difficult to wave solder, but can be placed on the wave-side (bottom) of the board if necessary. Doing so, however, may result in the need for rework.
   1. ICs (no less than 50 mil pitch)
      a. If it is necessary to place SOICs on the wave-side of the assembly, contact TAI for the recommended orientation and "thief-pad" layout.
   2. Resistor networks
   3. TVSP diodes
   4. C size, D size and larger tantalum capacitors
   5. SOT-23s
      a. Contact TAI for the preferred pad layout.
   6. Dpaks

D. If the following SMT parts are placed on the wave-side of a board, the board can be wave soldered by using selective pallets.
   1. Coils
   2. Electrolytic capacitors
   3. SOICs less than 50 mil pitch
   4. Connectors and sockets
   5. Switches
   6. Crystals with metal covers
   7. BGAs
   8. QFPs

   Note It is possible to wave solder certain QFPs if the QFP is placed on a 45° angle to the wave flow and pads act as solder thieves. This approach has been confirmed for QFPs down to 0.5mm pitch.
   9. Relays
   10. 0402 or smaller SMT components
   11. Components that cannot be subjected to heat greater than 250º C / 482º F

II. Spacing

A. The minimum pitch for SMT ICs is 0.012".

B. It is preferable that pads for 0.5mm pitch components be as wide as possible without violating spacing requirements. A pad width of 0.0107" is ideal.**-Mask dams should be maintained between all SMT pads, between all SMT pads and other unmasked areas (Pads, holes, vias, gnd planes, etc).**

C. Consistent center-to-center land spacing for all gull-wing and BGA components is requested.

Applicable to both SMT and Through-hole

I. Components

A. It is preferable to use parts that can be cleaned in an aqueous wash.

B. Standard sizes and values of parts are preferred.

1. For example, if using 10K parts, it is best to standardize the assembly with 1% tolerance components rather than use some with 1% tolerance and others with 5%.
2. For example, if using the same value component, it is best to standardize the assembly with one size rather than use two different sizes

C. On new designs, if possible, use components that are being used on current assemblies.

D. TAI would prefer to wave solder mixed-technology assemblies. Do not place non-wave-able SMT components on the wave-side of the assembly.

II. Polarity

A. It is preferable for all polarized components to be oriented in the same direction.

1. Polarities should face all left, all right, all up, or all down, if possible.

B. Ensure polarity markings are available in the CAD information, and on silk layer shown on the board**.**

C. Designating Polarity

1. Land patterns for components that can be electrically connected only one way must have some way of designating polarity.
2. The polarity marking on each component must be visible even after the component is mounted to aid QC during inspection
3. The following list indicates the typical ways to designate polarity on certain components. A minimum of one method is required. Use of all the methods is preferred.
   a. Through-hole DIPs
      i. Through-hole DIPs should have a "1" or a dot in the silk screen next to Pin 1.
      ii. All pads of the DIP should be round except for the pad of Pin 1, which should be square.
   b. Through-hole connectors
      i. Through-hole connectors should have a "1" in the silk screen next to Pin 1.
      ii. All pads of the connector should be round except for the pad of Pin 1, which should be square.
      iii. For connectors with more than one row, Pin 2 or the last pin of the connector should be designated as to how the pins are numbered.
   c. Through-hole polarized capacitors
      i. Through-hole capacitors should have a "+" in silk screen next to the positive pin's pad.
      ii. The positive pin's pad should be square while the negative pin's pad should be round.
   d. Through-hole diodes and LEDs
      i. Through-hole diodes and LEDs should have the cathode (-) end designated with a bar in the silk screen.
      a) Remember that the bar should be visible even after the diode or LED is soldered to the board.
      ii. The cathode (-) pin's pad should be square while the anode (+) pin's pad should be round.
   e. Through-hole SIPs

i. Pin 1 should be designated in the silk screen with a bar in between the pads of Pin 1 and Pin 2, or a dot next to the pad of Pin 1.
ii. Pin 1's pad should be square while the other pads should be round.

f. Through-hole transistors
i. The emitter pin should be designated in the silk screen with an "E".
ii. The outline of the part should be illustrated in the silk screen.

g. Through-hole batteries
i. Positive pins should have their pads designated with a "+" in the silk screen.
ii. The positive pin's pad should be square and the negative pin's pad, round.

h. Through-hole canister-type transistors or ICs
i. Canister-type components usually have a tab on the rim of the can to designate Pin 1
a) This tab should be shown on the silk screen to designate the mounting orientation.

j. SMT DIPs
i. The silk screen should include a "1" or a dot next to Pin 1.

k. SMT connectors
i. Surface mount connectors should have a "1" in the silk screen next to Pin 1. Pin 2 or the last pin needs to be designated to show how the pins are numbered if it is not obvious.

l. SMT polarized capacitors
i. Surface mount polarized capacitors should have the positive pad designated with a bar or "+" in silk screen.
NOTE: Remember that the bar designates positive instead of negative.

m. SMT diodes and LEDs
i. The cathode (-) end should be designated with a bar in the silk screen.
NOTE: Remember that the bar designates negative instead of positive.
a) For LEDs, a "-" and "+" in the silk screen sometimes are more helpful.

4. Whenever possible the CAD, number the pins/pads of your connectors and odd components the same way the manufacturer of that component numbers them.
a. This is very important when designing cables or pining out connectors, as it will greatly reduce error and confusion when assembling cables and trouble-shooting boards.

Through-hole

I. Lead Spacing

A. Consistent center-to-center lead spacing on axial leaded components.

B. Recommended spacing between DIP parts:

1. The side-to-side distance should be at least 0.100".
2. The top-to-top distance should be at least 0.050

II. Component Placement

A. It is preferable for DIP package parts to be more than ½" from the edge of the board.

B. No through-hole components should be placed on the wave-side (bottom) of the assembly whenever possible.

III. Auto Insertion

A. For through-hole boards that will run on axial and/or dip insertion machines, two (2) tooling/datum holes are required. These holes should be:

1. On the same long edge of the board
2. Minimum diameter of 0.125", maximum diameter of 0.250"
3. On X axis: minimum 0.125" from edge of board, maximum 0.250"
4. On Y axis: minimum .0125" from edge of board, maximum 0.300"

B. Locate the vias so that the leads of components installed by axial or dip insertion machines will not be located directly above or close to the via.

1. Shorting will occur between the component lead and via hole during the wave solder process if the two are too close together.

IV. Test Points

A. Test point pads must be a minimum of 0.030" in diameter and at least 0.050" center-to-center away from each other.
B. Make sure the test point pads are accessible after the board is assembled.
C. To keep test fixtures and testing costs down, place all test points on the same side of the board, as far away from each other as possible, and keep pad diameters as large a possible.

V .Eliminating Risk

A. If a connector consistently experiences shorting in the wave solder process, TAI may ask for permission to add "solder thieves" to the board to alleviate the solder shorts.

1. This is particularly true for component leads that have a square pad on the trailing edge of the PCB while going through the wave.
   NOTE: A "solder thief" is an additional solder land on a surface mount or through-hole assembly board. It is not electrically connected to any traces or pads and is positioned to follow the last component mounting land through a wave solder machine. Its purpose is to prevent solder accumulation and bridging.

B. Do NOT design wires (except jumper wires) to be soldered directly onto a circuit board.

1. Instead, use an insulation displacement connector or crimp a terminal on the end of the wire.

C. If possible, eliminate all jumper wires.

1. If jumper wires are necessary, use standard lead spacing and zero ohm resistors.

Printed Circuit Board (PCB)

I. Fiducials

A. TAI requires a minimum of two round fiducials per assembly side.

1. The fiducials should be across from each other, in opposite corners at non-symmetrical points.
   a. Ideally there should be three or four fiducials per side.
2. If the board is placed in an array, fiducials are required on both the assembly and rails.
3. Two different sizes of fiducials should be used per side.
   a. The two ideal fiducial sizes are:
      i. A 0.065" dia. pad with a 0.095" or larger dia. of Soldermask clearance, on rails.
      ii. A 0.050" dia. pad with a 0.080" or larger dia. of Soldermask clearance, on assembly.
4. If space permits, local fiducials should be added for fine pitch components (in addition to the three general fiducials for the board). Local fiducials reduce the possibility for misplacement, particularly for larger boards.

II. Rails

A. Rails are required for handling purposes for boards that have parts placed within 1/8" of the edge.
B. PCBs with SMT components or under 3” may require rails.
   1. The minimum rail width is .250", but a width of 0.3 - 0.5" is preferred.
C. Any board on which a component overhangs the edge needs a rail to extend a minimum of 0.125" past the farthest edge of the component.
D. PCBs with through-hole components to be inserted by an auto-insertion machine must have rails.
   1. The minimum rail width is 0.375".

III. Silk screen

A. Use a silk screen outline on the board to indicate the preferred location of test stamps, serial number labels, and other required stamps or labels.
B. The silk screen of polarized devices should be designed so that it is not covered after the components are placed.
C. A line width of 0.010" is preferred for component outlines.
D. A typical minimum readable text size is 0.060" character height using a .008" line width.
F. Silk screens should never be placed on top of an exposed pad. – any that are should be removed by the board house.
G. A minimum of 0.010" spacing is recommended between the silk screen and pads

IV. Pads

A. The optimum pad diameter for a through-hole component is twice its finished hole diameter.

V. Trace Width and Conductor Spacing

A. The minimum conductor spacing and trace width for 1 oz. finished copper is 0.007".

VI. Finished Hole Sizes

A. To determine optimum finished hole sizes for leads:
1. For components to be placed by TAI's auto-insertion equipment:
   a. Hole sizes should be 0.016" larger than the maximum lead for axial parts.
   b. Hole sizes should be 0.019" larger than the maximum lead for radial parts.
   c. Hole sizes should be 0.014" larger than the effective diameter of the lead for DIP parts.
2. For components to be hand placed:
   a. To determine optimum finished hole sizes for leads, add 0.008" to the maximum possible lead diameter.

B. Be sure to verify the calculations for the effective diameter of square post leads, as they can be deceiving - for example, the effective diameter of a 0.025" square post header is 0.035".

VII. Thermal Relief

A. Appropriate thermal reliefs should be used to connect a component lead to a plane or copper pour.
1. Examples are power or ground planes.

B. The total cumulative copper web for all layers connected to a plated through-hole should not exceed 0.160" for 1 oz. copper or 0.080" for 2 oz. copper.
C. For high-current applications (6 amps or more), thermal reliefs may not be applicable and wave or reflow soldering is recommended.

VIII. Vias

A. Do not place exposed vias underneath 0805 or smaller chip components.
B. Do not place vias in SMT pads.
1. Two exceptions to this guideline is when vias are used for heat sinking under power ICs.
2. If vias in pads are necessary, contact TAI for information on the repercussions that may result.

C. Place vias so that leads of components installed by axial or dip insertion machines will not be located directly above or close to the via.
1. Shorting will occur between the component lead and via hole during the wave solder process if the two are too close together.

D. The via pad diameter should be 0.020" larger than the diameter of the finished hole for that via.

E. Verify that the cross-sectional area of a via is equal to or greater than the cross-sectional area of the trace connected to it.
1. See the "Trace widths vs. Via Sizes" section of this document for the formulas used to calculate cross-sectional area.

F. Fan-out vias under BGAs
1. To reduce the chance of solder shorts on wave soldered boards that have BGAs, remove the soldermask openings on the wave side of the fan-out vias that are under BGAs. In other words, cap the vias with soldermask.

IX. Soldermask

A. The typical soldermask has a 0.005" annular ring around every pad except fiducials.

1. For example, if the component pad is 0.060" diameter, then its soldermask should be 0.070" diameter.

B. For fine pitch components (0.5 mm pitch with 0.009" space between pads) use a 0.003" annular ring.

C. If vias are closely clustered, reduce the soldermask opening for the vias to eliminate the risk of shorting between vias in the wave solder process.

D. Soldermask web is preferred between SMT pads and vias. The minimum web must be 0.003" wide.

X. Trace Widths vs. Via Sizes

A. The cross-sectional area of a via should be equal to or greater than the cross-sectional area of the trace connected to it.

1. Maximizing cross-sectional area of vias helps prevent high-speed transmission line glitches, via blowouts and reduces overall circuit resistance.

B. Use this formula to determine the cross-sectional area of a trace:

1. (Trace width) x (Copper thickness) = Cross-sectional area of trace
   a. Typical copper thickness for ½ oz. copper = 0.00072"
   b. Typical copper thickness for 1 oz. copper = 0.0014"
   c. Typical copper thickness for 2 oz. copper = 0.0028"
   d. Typical copper thickness for 3 oz. copper = 0.0043"

C. Use this formula to determine the cross-sectional area of a via plated up 0.001" inside the hole:

1. (0.7854) x (D + 0.002") x (D + 0.002") - (0.7854) x (Dx (D) = Cross-sectional area of via
   a. D = diameter of finished via hole expressed in inches
   b. 0.001" plating inside holes is the typical minimum-plating requirement for TAI.

XI. Board Outline/Edges

A. Line Width

1. A 0.010" line width should be used to draw the board outline

B. When creating Gerber files for manufacturing, the board outline should be included on every layer to provide common features for alignment.

C. Keep copper traces a minimum of 0.010" away from routed edges and 0.020" away from V-scored edges.

D. Discrete SMT components should be a minimum of 0.030" away from board edges that are V-scored or have breakaway tabs.

1. Components closer than 0.030" to board edges may crack during depanelization.

F. Providing the connector clearance will allow it, "V-score" is preferable to breakaway-tabs.

G. If the PCB size is expected to be larger than 8" x 10", contact TAI to obtain the optimum recommended board size for efficiency of fabrication.

XII. Review

A. A manufacturing design review is strongly recommended before boards are fabricated.